Remarks

I. Status of claims

Claims 1-20 are pending.

The Examiner has indicated that claims 5-8, 13-14, 16, and 19-20 would be allowable if rewritten in independent form.

II. Claim rejections under 35 U.S.C. § 112

The Examiner has rejected claims 9-11 under 35 U.S.C. § 112, second paragraph, due to insufficient antecedent basis for certain terms.

The dependency of claim 9 has been corrected in a way that addresses the Examiner's § 112, second paragraph, concerns. Accordingly, the Examiner's rejection under 35 U.S.C. § 112, second paragraph, now should be withdrawn.

Claims 9-11 depend from claim 5 and therefore should be allowable for at least the same reasons as claim 5.

III. Claim rejections under 35 U.S.C. § 102

The Examiner has rejected claims 1-4, 12, 15, 17, and 18 under 35 U.S.C. § 102(e) over Bodley (U.S. 6,801,196).

A. Independent claim 1

Independent claim 1 recites:

> Claim 1 (original): A device, comprising:
>
> a sleep recovery circuit operable to transition from a first signal detection mode to a second signal detection mode in response to detection of a first signal characteristic in an input signal, and to transition from the second signal detection mode to a third operational mode in response to detection in the input signal of a second signal characteristic different from the first signal characteristic.

In support of the rejection of claim 1, the Examiner has stated that:

> Bodley teaches a device [*display device, see abstract*], comprising a sleep recovery circuit [*300 of Fig. 3*] operable to transition from a first signal detection mode [*low power mode 3 of Fig. 4*] to a second signal detection mode [*lower power mode 2*] in response to detection of a first signal characteristic [*logical high, col. 4, line 4*] in an input signal [*power control signal 214, see col. 4, lines 1-2*], and to transition from the second signal detection mode to a third operational mode [*Full power 0 of Fig. 4, col. 4, ,lines 26-30*] in response to detection in the input signal of a second signal characteristic different from the first signal characteristic [*logical low, col. 4, line 8*].

However, the embodiment 300 of Bodley's power control circuit 120 shown in FIG. 3 does not operate in the manner described by the Examiner in support of the rejection of claim 1. In particular, the power control circuit 300 does not transition from the low power mode 3 to the lower power mode 2 in response to detection of a logical high voltage level in the power control signal P that is provided on the signal path 214, nor does the power control circuit 300 transition from the lower power mode 3 to the full power mode 0 in response to detection of a logical low voltage level in the power control signal P. As explained in detail below, the power control circuit 300 is not responsive to the power control signal P on the power control signal path 214. In addition, it is the *display device 128* that transitions from the state 3 to the state 2 in response to the transition of the power control signal P on the power control signal path 214 from OFF (logical low) to ON (logical high), and transitions from the state 2 to the state 0 in response to the detection that the data signal 210 or the control signal 212 is in the active state while the power control signal P is ON.

As shown clearly in FIG. 2, the signal path 214 is not connected to the power control circuit. In accordance with Bodley's teachings, "Signal path 214 provides a path by which a power control signal may be applied to electronic switch 218 to disconnect power to internal power signal path 216" (col. 3, lines 37-40). When the power control signal P is ON, the switch 218 is closed allowing power to be delivered to components of the display device 128 if the mechanical switch 118 also is closed (see col. 4, lines 3-6). When the power control signal P is OFF, the switch 218 is open preventing power to be delivered to components of the display device 128 regardless of the state of the mechanical switch 118 (see col. 4, lines 6-10).

The power control circuit 300, on the other hand, is responsive to only a single characteristic (i.e., the signal activity rate) of the signal on the data signal path 212 or the signal on the control signal path 210. In particular, the power control circuit 300 includes an activity monitor 310 that "examines the rate of signaling on the data signal path 212, or the signaling rate of certain control signal path (such as the rate of a clock or sync signal)" (col. 3, lines 45-47). The activity monitor 310 transmits an indication signal to the control logic circuit 312 when the monitored signal activity rate falls below a predefined threshold level (see col. 3, lines 48-51, and FIG. 3). In response to the indication signal transmitted by the activity monitor 310, the control logic circuit 312 provides a signal 308 that reduces power consumption by other components of the display device 128 (see col. 3, lines 53-56). In response to a signal received from a timer circuit 314, which tracks the duration of the low-activity state detected by the activity monitor 310, the control logic circuit 312 provides a signal 309 that reduces power consumption in other components of the display device 128 (see col. 3, lines 57-67).

FIG. 4 shows the different power states of the display device 128. The transitions between the power states of the display device 128 are determined by three factors: the state of the power control signal P, which is controlled by an application program executing on the computer system 126 (see col. 4, lines 51-54), and the states of the power control signals 308, 309 both of which depend on the detection of the low-activity state in the data signal 210 or the control signal 212 by the power control circuit 300. In particular, the transition from state 0 to state 1 occurs when the power control signal 308 is activated (i.e., the low-activity state of the data signal 210 or the control signal 212 is detected). The transition from state 1 to state 2 occurs when both the power control signals 308, 309 are activated (i.e., the low-activity state of the data signal 210 or the control signal 212 is detected and persists longer than a predetermined threshold). If the power control signal P is turned OFF (logical low) during any of the states 0-2, a transition is made to the lower power state 3 (see col. 4, lines 30-33). According to Bodley, "Display device 128 remains in state 3 until P is turned 'ON' again (no longer applied), at which time a transition is made to state 2" (col. 4, lines 36-39). The transitions to and from states 4 and 5 depend on the state of the manual power switch 118, as described in col. 4, lines 40-47.

In summary, the power control circuit 300 does not transition to different states based on the detection of the logical high and logical low states of the power control signal P on the

power control signal path 214 as proposed by the Examiner. Instead, the power control circuit 300 *detects* only a single characteristic of the data signal 210 or the control signal 212: namely, the signaling rate, which is used to determine whether the data signal 210 or the control signal 212 is in the low activity state or the active state. The power control circuit 300 provides the power control signal 308 to certain components of the display device 128 in response to the detection of the low activity state and provides the power control signal 309 to certain other components of the display device 128 in response to the persistence of the detected low activity state beyond a predetermined threshold duration.

In summary, the display device described in Bodley does not transition from a first detection mode to a second detection mode and from the second detection mode to a third operational mode in response to the detection of different respective signal characteristics in the same input signal as recited in claim 1. In the exemplary state transition sequence cited by the Examiner, the transitions from the state 3 to state 2 and from state 2 to state 0 involve the detection of the same signal characteristic in the power mode control signal P on signal path 214: namely, the detection of the logical high state. The transition from state 2 to state 0 also involves the detection of a single characteristic (i.e., the signaling rate) in the data signal 210 or the control signal 212, both of which are different from the power mode control signal P on signal path 214.

For this reason, the Examiner's rejection of independent claim 1 under 35 U.S.C. § 102(e) over Bodley should be withdrawn.

B. Claims 2-4, 12, 15, and 17

Each of claims 2-4, 12, 15, and 17 incorporates the features of independent claim 1 and therefore is patentable over Bodley for at least the same reasons explained above.

C. Independent claim 18

Independent claim 18 recites features that essentially track the pertinent features discussed above in connection with independent claim 1 and, therefore, is patentable over Bodley for at least the same reasons explained above.

IV. Conclusion

For the reasons explained above, all of the pending claims are now in condition for allowance and should be allowed.

Charge any excess fees or apply any credits to Deposit Account No. 50-3718.

Respectfully submitted,

Date: April 22, 2006

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